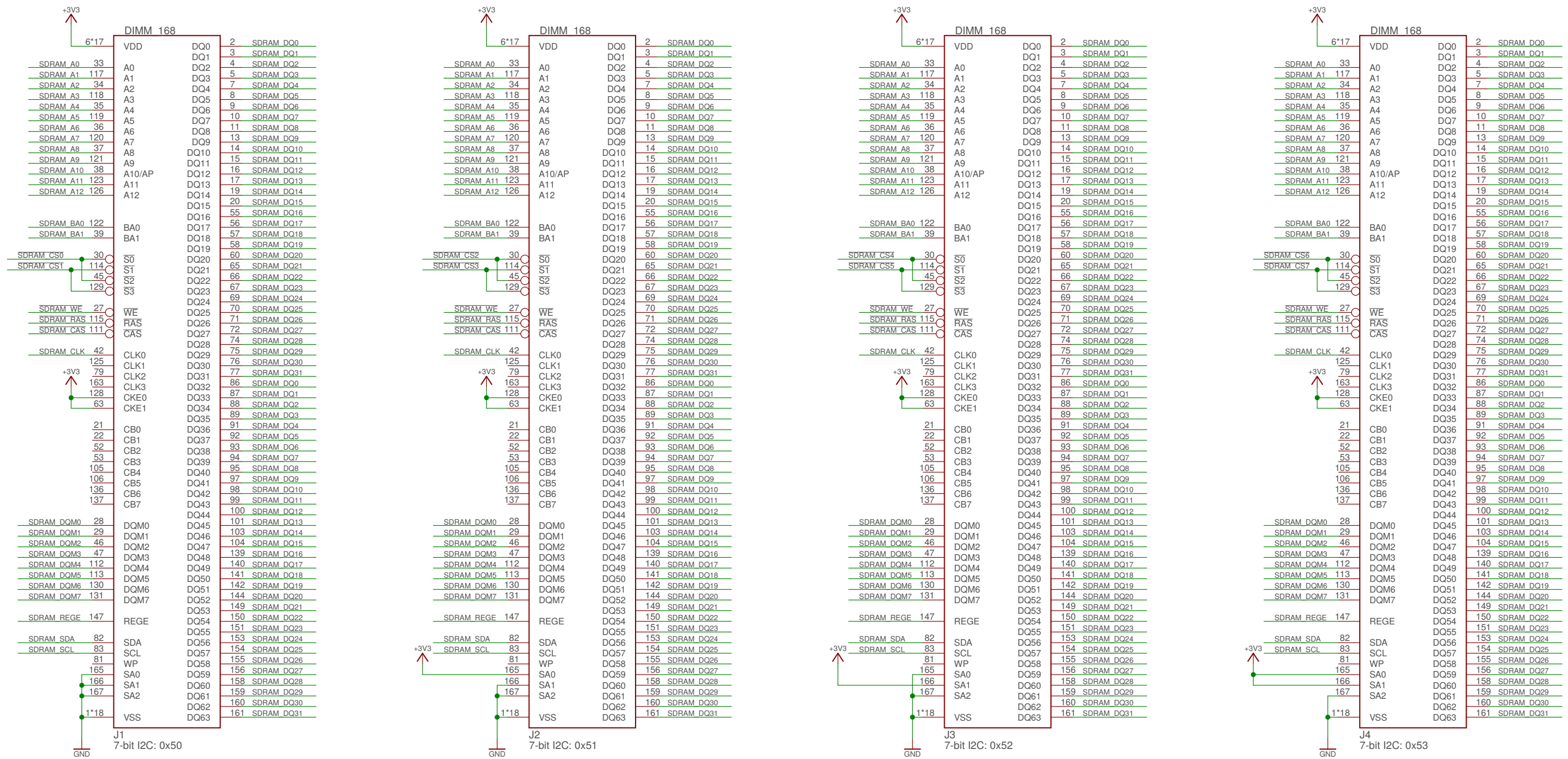
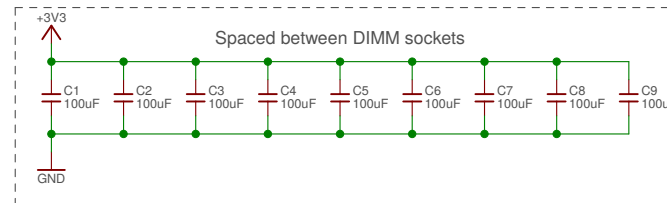


4x 168-pin SDR SDRAM PC66/100/133 DIMM Sockets

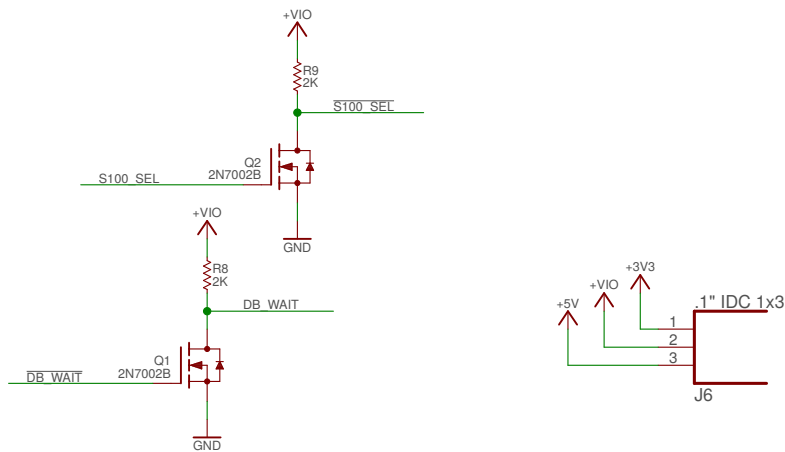
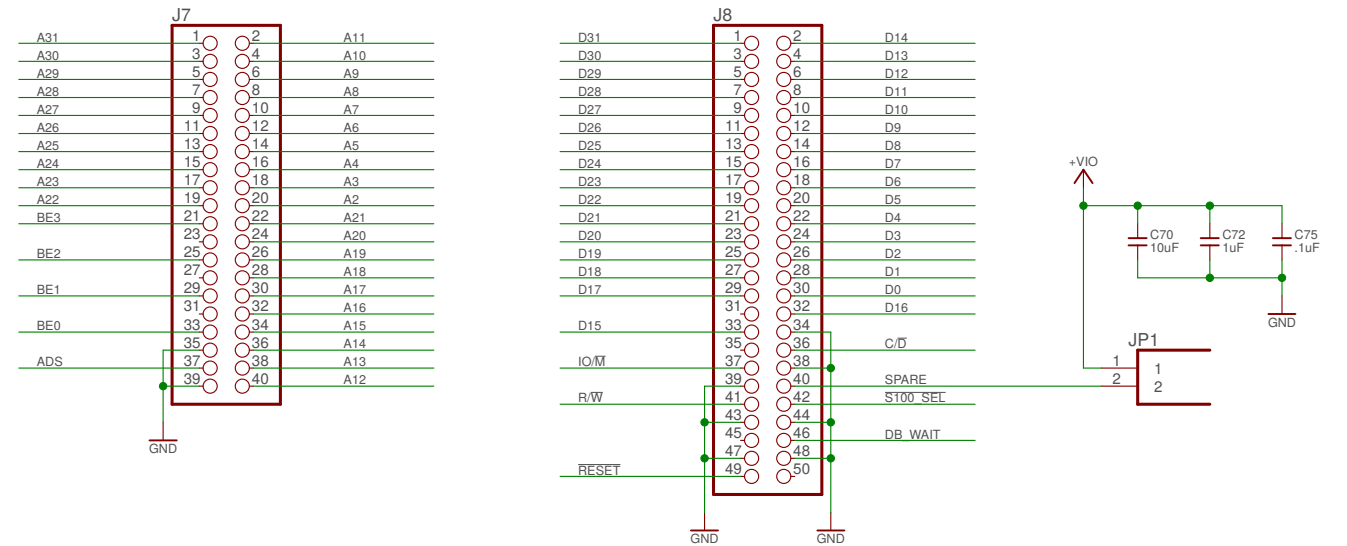
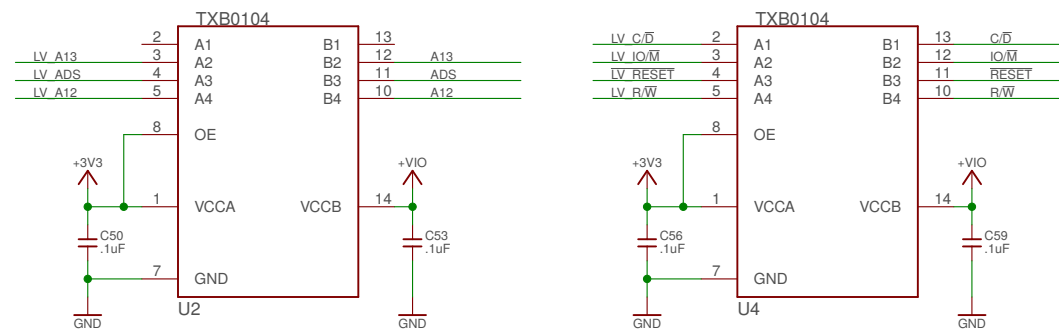
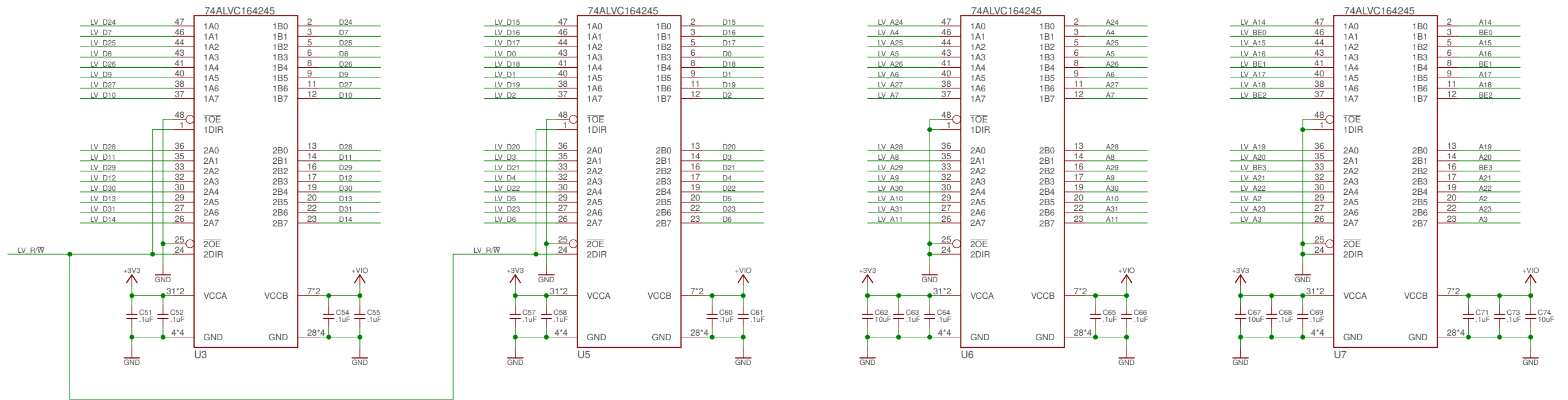


1 or 2 physical banks per DIMM
 13 row address, 12 column address, 2 bank address (27 address bits)
 2 sets of DQMs for folded over data lines (1 address bit)
 4 byte enables -> DQMs (2 address bits)



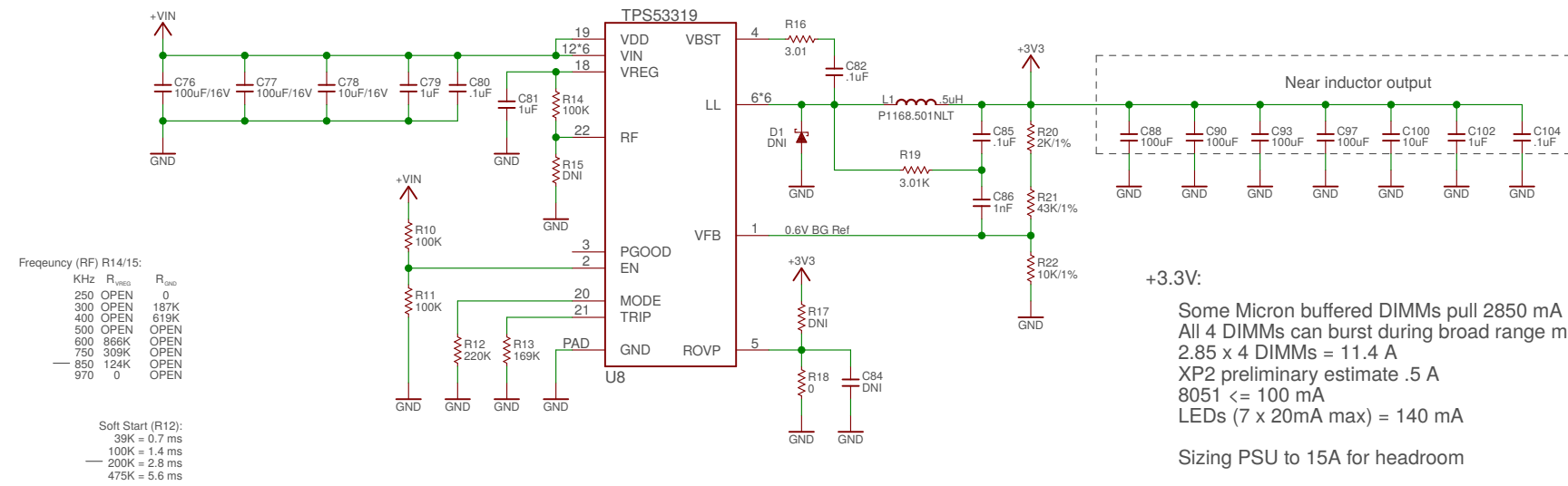
<h2>4 GB S100 Memory Board</h2>	
TITLE: SDRAM_4G_s100	
Document Number:	REV: P2
Date: 4/7/17 1:36 PM	Sheet: 1/5

VIO -> 3.3V Translation and Overhead Host Bus

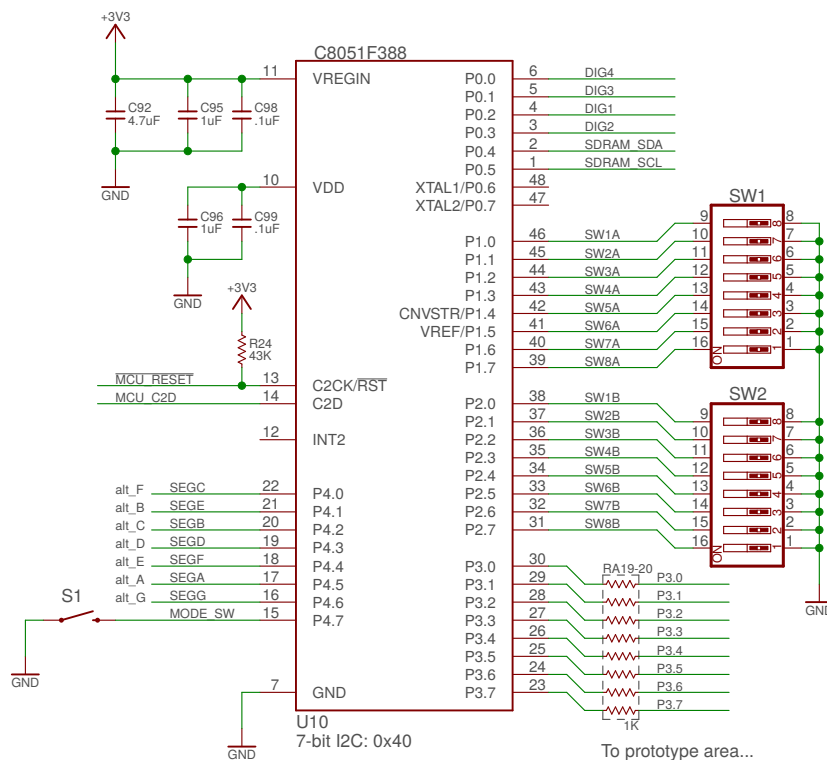
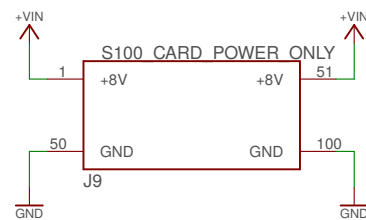
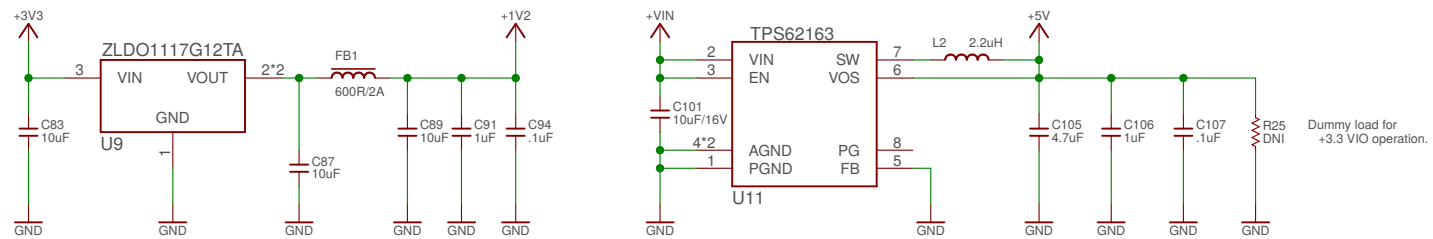
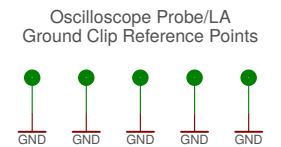
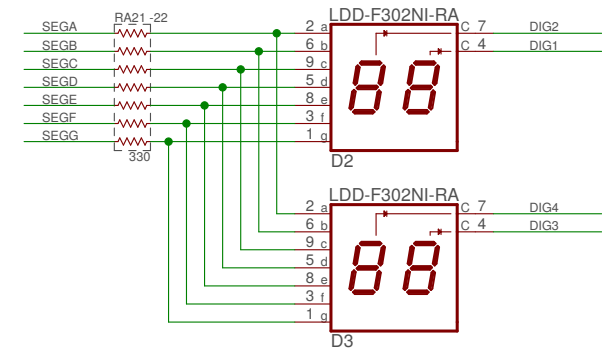


<h2>4 GB S100 Memory Board</h2>	
TITLE: SDRAM_4G_s100	
Document Number:	REV: P2
Date: 4/7/17 1:36 PM	Sheet: 3/5

3.3V @ 15A, 1.2V @ 1A, 5V @ 1A PSU / MCU I2C Expander



+3.3V:
 Some Micron buffered DIMMs pull 2850 mA in burst operation
 All 4 DIMMs can burst during broad range memset's
 2.85 x 4 DIMMs = 11.4 A
 XP2 preliminary estimate .5 A
 8051 <= 100 mA
 LEDs (7 x 20mA max) = 140 mA
 Sizing PSU to 15A for headroom



4 GB S100 Memory Board

TITLE: SDRAM_4G_s100

Document Number: _____ REV: P2

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