PAL Equations of PC532

This document contains the descriptions of the six PAL for the PC532.

Content:

NOTE from Pell: As updates for the PALs, I've only gotten the PLD files
from George. Thus, you have to generate the corresponding JEDEC file
yourself. Unfortunately I cannot handle this PAL syntax (only ABEL and A-PLUS)
so I cannot help you with this. If you generate new JEDEC files then please
send them to pell@isy.liu.se. Thanks!

----- BEGIN CHANGES -----

The changes to the parity pal are to ensure that /NMI is asserted and
remains asserted after a power on reset. Software can then clear the /NMI
when it is good and ready by reading from /PARITYCL. The 32532 only detects
an /NMI when it sees a high to low transition, hence having /NMI asserted
at reset is ok. We had to do this 'cos for some reason if /NMI blips up
and down during the reset period the 32532 gets 'depressed'! The changes
to the DEC32 pal are to do with enabling the 74as646 during a psuedo-dma
access to the SCSI port. We still have to check the SCSI out fully on this
new rev pcb, but so far things look very good, i.e. no cuts or jumpers yet.

--
George Scolaro
george@wombat
(try {pyramid|sun|vsi1|killer} !daver!wombat!george) [37 20 51 N / 122 03 07 W]

```
*******************************************************************************
                                    dec32
*******************************************************************************

CUPL            3.00 Serial# MD-300-5631
Device          p16l8  Library DLIB-h-24-8
Created         Sun Dec 10 19:14:21 1989
Name            dec32
Partno
Revision        01
Date            05/12/88
Designer        George Scolaro
Company         George Scolaro
Assembly        32532 PC/AT board
Location

===============================================================================
                            Expanded Product Terms
===============================================================================

dram =>
    !a27 & !a28 & !a29 & !a30 & !a31 & !swap
  # a27 & !a28 & !a29 & !a30 & !a31 & swap

duart =>
    a27 & !a28 & a29 & !a30 & !a31 & !ioinh

eprom =>
    !a27 & !a28 & !a29 & !a30 & !a31 & conf & swap
  # !a27 & a28 & !a29 & !a30 & !a31 & conf

icu =>
    !a08 & a27 & a28 & a29 & a30 & a31 & conf & !ioinh

iodec =>
    !a27 & a28 & a29 & !a30 & !a31 & conf
  # !a28 & a29 & !a30 & !a31 & conf
  # !a08 & a27 & a28 & a29 & a30 & a31 & conf

memadr =>
    a31 , a30 , a29 , a28 , a27 , a08

scsi =>
    !a27 & a28 & a29 & !a30 & !a31 & !ioinh
  # a27 & a28 & a29 & !a30 & !a31

slow =>
    !a27 & !a28 & !a29 & !a30 & !a31 & swap
  # !a27 & a28 & !a29 & !a30 & !a31
  # a27 & !a28 & a29 & !a30 & !a31 & !ioinh
  # !a27 & a28 & a29 & !a30 & !a31 & !ioinh
  # !a08 & a27 & a28 & a29 & a30 & a31 & !ioinh

slows =>
    !a27 & !a28 & !a29 & !a30 & !a31 & swap
  # !a27 & a28 & !a29 & !a30 & !a31
  # a27 & !a28 & a29 & !a30 & !a31 & !ioinh
  # a28 & a29 & !a30 & !a31 & !ioinh
  # !a08 & a27 & a28 & a29 & a30 & a31 & !ioinh
```

```
dram.oe  =>    1

duart.oe  =>   1

eprom.oe  =>   1

icu.oe  =>     1

iodec.oe  =>   1

scsi.oe  =>    1

slow.oe  =>    1

slows.oe  =>   1
```

Symbol Table

Pin Pol	Variable Name	Ext	Pin	Type	Pterms Used	Max Pterms	Min Level
	a08		7	V	-	-	-
	a27		5	V	-	-	-
	a28		4	V	-	-	-
	a29		3	V	-	-	-
	a30		2	V	-	-	-
	a31		1	V	-	-	-
!	conf		9	V	-	-	-
!	dram		15	V	2	7	1
!	duart		18	V	1	7	1
!	eprom		14	V	2	7	1
!	icu		17	V	1	7	1
!	iodec		12	V	3	7	1
!	ioinh		8	V	-	-	-
	memadr		0	F	-	-	-
	nc0		11	V	-	-	-
!	scsi		16	V	2	7	1
!	slow		19	V	5	7	1
!	slows		13	V	5	7	1
	swap		6	V	-	-	-
	dram	oe	15	D	1	1	0
	duart	oe	18	D	1	1	0
	eprom	oe	14	D	1	1	0
	icu	oe	17	D	1	1	0
	iodec	oe	12	D	1	1	0
	scsi	oe	16	D	1	1	0
	slow	oe	19	D	1	1	0
	slows	oe	13	D	1	1	0

LEGEND F : field D : default variable M : extended node
N : node I : intermediate variable T : function
V : variable X : extended variable U : undefined

```
Name            dramc;
Partno          ;
Date            05/14/88;
Revision        03;
Designer        George Scolaro;        /* (C) 1988,89,90 */
Company         George Scolaro;
Assembly        32532 PC/AT board;
Location        U39;
Device          p16r8;

/*************************************************************************/
/* This pal generates ras/cas timing for all dram accesses including:  */
/* - cas before ras refresh (with precharge before & after refresh)    */
/* - page miss with re-ras, rea or write (with precharge)              */
/* - page hit with cas access (for write)                              */
/* - page hit with cas access (for read, burst access)                 */
/*************************************************************************/
/*  Allowable Target Device Types:       PAL16R8D                      */
/*************************************************************************/

/**  Inputs  **/

Pin   1     = bclk          ; /* 32532 system clock */
Pin   2     = !dram         ; /* dram select */
Pin   3     = !conf         ; /* 32532 bus cycle confirmed */
Pin   4     = !hsa          ; /* high speed access in progress */
Pin   5     = !rfrqin       ; /* refresh request */
Pin   6     = !bout         ; /* burst access request */
Pin   7     = !bmt          ; /* begin memory transfer */
Pin   8     = !ddin         ; /* data direction from 32532 */
Pin   9     = nc0           ; /* */
Pin   11    = !oe           ; /* enable pal */

/**  Outputs  **/

Pin   12    = !ras          ; /* ras to rams */
Pin   13    = !cas          ; /* cas to rams */
Pin   14    = !rfcyc        ; /* refresh in progress */
Pin   15    = !rfrq         ; /* synchronized refresh request */
Pin   16    = !nrdyr        ; /* not ready to 32532 */
Pin   17    = !da           ; /* internal counter */
Pin   18    = !casp         ; /* cas parity clock */
Pin   19    = !rfdone       ; /* refresh complete */

/** Declarations and Intermediate Variable Definitions **/

field output =  [ras, cas, rfcyc, da];

$define idle      'b'1000

$define prech1    'b'0000
$define prech2    'b'0001

$define accw      'b'1001
$define acc1      'b'1100
$define acc2      'b'1101

$define ref1      'b'0011
$define ref2      'b'0111
$define ref3      'b'1111
$define ref4      'b'1011
```

```
$define ref5      'b'0010
$define ref6      'b'0110
$define ref7      'b'1110
$define ref8      'b'1010

/**  Logic Equations  **/

rfrq.d = rfrqin & !rfdone     /* synchronise the external refresh request */
       # rfrq & !rfcyc;

rfdone.d = rfcyc              /* refresh done for this rfrqin */
         # rfdone & rfrqin;

nrdyr.d = dram & bmt & !hsa   /* always when not a high speed access */
        # dram & bmt & rfrq   /* start of any dram access if refresh */
        # dram & (bmt # conf) & rfcyc     /* during refresh cycle */
        # output:[prech1] & dram & conf
        # output:[prech2] & dram & conf
        # output:[acc2] & bout
        # output:[accw] & !(hsa & !bout) & ddin;

sequence output {

present idle
        if !rfrq & hsa & dram & bmt & ddin      /* read access has no wait */
                next accw out casp;
        if !rfrq & hsa & dram & bmt & !ddin     /* write access has no wait */
                next acc2;
        if !rfrq & !hsa & dram & bmt
                next prech1;
        if rfrq
                next ref1;
        default
                next idle;

present acc1
        if ddin
                next acc2 out casp;
        if !ddin
                next idle;

present acc2
        if bout
                next acc1;
        if !bout
                next idle;

present prech1
        next prech2;

present prech2
        if rfrq & !(dram & (conf # bmt))
                next ref2;
        if dram & (conf # bmt)
                next accw;
        default
                next prech2;
```

```
present accw
        if hsa & !bout        /* 0 wait state access if in page and not */
                next idle;    /*  a burst access */
        default
                next acc1;

present ref1
        next ref2;

present ref2
        next ref3;

present ref3
        next ref4;

present ref4
        next ref5;

present ref5
        next ref6;

present ref6
        next ref7;

present ref7
        next ref8;

present ref8
        next prech1;
}
```

```
********************************************************************************
                                    dramen
********************************************************************************

CUPL            3.00 Serial# MD-300-5631
Device          p2018  Library DLIB-h-24-8
Created         Sun Dec 10 19:17:56 1989
Name            dramen
Partno
Revision        01
Date            05/07/88
Designer        George Scolaro
Company         George Scolaro
Assembly        32532 PC/AT board
Location        U19

================================================================================
                            Expanded Product Terms
================================================================================
bank0 =>
    !banks & !ras
  # bank0 & !bank1
  # rfcyc

bank1 =>
    banks & !ras
  # !bank0 & bank1
  # rfcyc

cas0 =>
    cas & rfcyc
  # be0l & cas & !ddin
  # bmt & conf & ddin & hsadr & ras & !rfcyc & !rfrqi
  # !cas & cas1 & conf & ddin & hsadr & !rfcyc
  # cas & ddinl & qo0
  # cas & ddinl & qo1

cas1 =>
    cas & rfcyc
  # be1l & cas & !ddin
  # bmt & conf & ddin & hsadr & ras & !rfcyc & !rfrqi
  # !cas & cas1 & conf & ddin & hsadr & !rfcyc
  # cas & ddinl & qo0
  # cas & ddinl & qo1

cas2 =>
    cas & rfcyc
  # be2l & cas & !ddin
  # bmt & conf & ddin & hsadr & ras & !rfcyc & !rfrqi
  # !cas & cas1 & conf & ddin & hsadr & !rfcyc
  # cas & ddinl & qo0
  # cas & ddinl & qo1

cas3 =>
    cas & rfcyc
  # be3l & cas & !ddin
  # bmt & conf & ddin & hsadr & ras & !rfcyc & !rfrqi
  # !cas & cas1 & conf & ddin & hsadr & !rfcyc
  # cas & ddinl & qo0
  # cas & ddinl & qo1
```

```
bank0.oe  =>   1

bank1.oe  =>   1

cas0.oe  =>    1

cas1.oe  =>    1

cas2.oe  =>    1

cas3.oe  =>    1

ras.oe  =>     0

rfrqi.oe  =>   0
```

Symbol Table

Pin Pol	Variable Name	Ext	Pin	Type	Pterms Used	Max Pterms	Min Level
!	bank0		19	V	3	7	1
!	bank1		16	V	3	7	1
	banks		8	V	-	-	-
!	be0l		1	V	-	-	-
!	be1l		2	V	-	-	-
!	be2l		3	V	-	-	-
!	be3l		4	V	-	-	-
!	bmt		6	V	-	-	-
!	cas		7	V	-	-	-
!	cas0		15	V	6	7	1
!	cas1		17	V	6	7	1
!	cas2		18	V	6	7	1
!	cas3		22	V	6	7	1
!	conf		13	V	-	-	-
!	ddin		14	V	-	-	-
!	ddinl		23	V	-	-	-
!	hsadr		11	V	-	-	-
	qo0		9	V	-	-	-
	qo1		10	V	-	-	-
!	ras		20	V	-	-	-
!	rfcyc		5	V	-	-	-
!	rfrqi		21	V	-	-	-
	bank0	oe	19	D	1	1	0
	bank1	oe	16	D	1	1	0
	cas0	oe	15	D	1	1	0
	cas1	oe	17	D	1	1	0
	cas2	oe	18	D	1	1	0
	cas3	oe	22	D	1	1	0
	ras	oe	20	D	1	1	0
	rfrqi	oe	21	D	1	1	0

```
LEGEND    F : field      D : default variable        M : extended node
          N : node       I : intermediate variable   T : function
          V : variable   X : extended variable       U : undefined
```

```
Name             parity;
Partno           ;
Date             891201;
Revision         02;
Designer         George Scolaro;        /* (C) 1989,90 */
Company          George Scolaro;
Assembly         32532 PC/AT board;
Location         U20;
Device           g20v8ms;

/*************************************************************************/
/* Parity checker pal. This pal takes the latched parity errors from   */
/* each byte as well as the latched byte enables and bank.             */
/* Parity errors detected during /CASP are clock on the next bclk edge */
/* and can then be read along with the offending bank. An /NMI is      */
/* generated when a parity error occurs. No further parity errors a    */
/* checked for until the software (optionally) reads the error latch   */
/* and then issues a /paritycl to clear the parity error latch and     */
/* deassert the /NMI.                                                  */
/*************************************************************************/
/*  Allowable Target Device Types:  GAL20V8A-15                        */
/*************************************************************************/

/**  Inputs  **/

Pin   1     = bclk           ; /* 32532 system clock */
Pin   2     = !casp          ; /* cas parity (from DRAMC) */
Pin   3     = !rsto          ; /* system reset */
Pin   4     = !banks    ; /* bank select signal */
Pin   5     = !be0lp    ; /* 4 clocked byte enables */
Pin   6     = !paritycl ; /* clear parity error latch */
Pin   7     = !pdi3p    ;
Pin   8     = !pdi1p    ;
Pin   9     = !pdi0p    ;
Pin   10    = !be3lp    ;
Pin   11    = !be1lp    ;
Pin   13    = !parityrd ; /* read data */
Pin   14    = !be2lp    ;
Pin   23    = !pdi2p    ; /* 4 bytes worth of parity information */

/**  Outputs  **/

Pin   15    = !bankc    ; /* clocked bank select signal */
Pin   16    = !cparity  ; /* parity check enable signal */
Pin   17    = !nmi           ; /* the actual parity error signal  */
Pin   18    = !bankl    ; /* latch bank select if parity error */
Pin   19    = !perr2    ;
Pin   20    = !perr0    ; /* parity error occurred on this byte */
Pin   21    = !perr1    ;
Pin   22    = !perr3    ;

/** Declarations and Intermediate Variable Definitions **/

/**  Logic Equations  **/

cparity.d = casp;
bankc.d     = banks;

nmi   = perr0                      /* async output */
      # perr1
      # perr2
```

```
      # perr3
      # rsto
      # nmi & !paritycl;

perr0.d     = pdi0p & be0lp & cparity & !nmi
      # perr0 & !(rsto # paritycl);

perr1.d     = pdi1p & be1lp & cparity & !nmi
      # perr1 & !(rsto # paritycl);

perr2.d     = pdi2p & be2lp & cparity & !nmi
      # perr2 & !(rsto # paritycl);

perr3.d     = pdi3p & be3lp & cparity & !nmi
      # perr3 & !(rsto # paritycl);

bankl.d     = bankc & pdi0p & be0lp & cparity & !nmi
      # bankc & pdi1p & be1lp & cparity & !nmi
      # bankc & pdi2p & be2lp & cparity & !nmi
      # bankc & pdi3p & be3lp & cparity & !nmi
      # bankl & !(rsto # paritycl);
```

```
*******************************************************************************
                                    scsi
*******************************************************************************

CUPL            3.00 Serial# MD-300-5631
Device          p16l8  Library DLIB-h-24-8
Created         Sun Dec 10 19:14:58 1989
Name            scsi
Partno
Revision        01
Date            07/25/88
Designer        George Scolaro
Company         George Scolaro
Assembly        32532 PC/AT board
Location        U40

===============================================================================
                            Expanded Product Terms
===============================================================================

ch0sel =>
    conf & select

ch1sel =>
    conf & !select

dack0 =>
    dack & select

dack1 =>
    dack & !select

drqs =>
    !drqs0 & !drqs1
  # !drqs1 & !select
  # !drqs0 & select

scsi0 =>
    !scsi
  # a27
  # !select
  # !conf

scsi1 =>
    !a27 & conf & scsi & !select

scsii =>
    !scsii0 & !scsii1
  # !scsii1 & !select
  # !scsii0 & select

scssel =>
    !a27 & scsi

dack0.oe  =>
    1

dack1.oe  =>
    1
```

```
drqs.oe  =>
    1

scsi0.oe  =>
    1

scsi1.oe  =>
    1

scsii.oe  =>
    1
```

==========

Symbol Table

==========

Pin Pol	Variable Name	Ext	Pin	Type	Pterms Used	Max Pterms	Min Level
	a27		9	V	-	-	-
	ch0sel		0	I	1	-	-
	ch1sel		0	I	1	-	-
!	conf		11	V	-	-	-
!	dack		6	V	-	-	-
!	dack0		17	V	1	7	1
!	dack1		16	V	1	7	1
	drqs		18	V	3	7	1
	drqs0		3	V	-	-	-
	drqs1		4	V	-	-	-
	nc0		7	V	-	-	-
	nc1		14	V	-	-	-
	nc2		15	V	-	-	-
!	scsi		8	V	-	-	-
	scsi0		13	V	4	7	1
!	scsi1		12	V	1	7	1
	scsii		19	V	3	7	1
!	scsii0		1	V	-	-	-
	scsii1		2	V	-	-	-
	scssel		0	I	1	-	-
	select		5	V	-	-	-
	dack0	oe	17	D	1	1	0
	dack1	oe	16	D	1	1	0
	drqs	oe	18	D	1	1	0
	scsi0	oe	13	D	1	1	0
	scsi1	oe	12	D	1	1	0
	scsii	oe	19	D	1	1	0

LEGEND F : field D : default variable M : extended node
        N : node I : intermediate variable T : function
        V : variable X : extended variable U : undefined

```
********************************************************************************
                                     wait
********************************************************************************

CUPL            3.00 Serial# MD-300-5631
Device          p16r6  Library DLIB-h-24-14
Created         Sun Dec 10 19:16:20 1989
Name            wait
Partno
Revision        1A
Date            1/14/89
Designer        George Scolaro
Company         George Scolaro
Assembly        32532 PC/AT board
Location        U38

================================================================================
                              Expanded Product Terms
================================================================================

da.d  =>
    da & !db & !dc & nrdy & scsi & !slow
  # bmt & !da & !db & !dc & !nrdy & slow
  # bmt & !da & !db & !dc & scsi & scsii
  # bmt & !da & !db & !dc & drq & scsi
  # !da & dc & nrdy
  # !da & db & nrdy
  # !da & nrdy & scsii
  # !da & drq & nrdy

dack =>
    iowr & scsi & !slow
  # iord & scsi & !slow

db.d  =>
    da & !db & nrdy
  # !da & db & nrdy

dc.d  =>
    da & !db & nrdy & scsi & !slow
  # da & db & !dc & nrdy
  # !da & db & nrdy & scsi
  # !db & dc & nrdy
  # !da & dc & nrdy

eop =>
    a22 & iowr & scsi & !slow
  # a22 & iord & scsi & !slow

iord.d  =>
    bmt & ddin & scsi & slow
  # db & !dc & ddin & nrdy
  # da & !db & ddin & nrdy
  # bmt & ddin & scsi & scsii
  # bmt & ddin & drq & scsi
  # !da & dc & ddin & nrdy
  # !da & ddin & nrdy & scsii
  # !da & ddin & drq & nrdy
```

```
iowr.d  =>
    !da & dc & !ddin & !drq & nrdy & !scsii
  # db & !dc & !ddin & nrdy
  # !da & !ddin & drq & nrdy & !scsii
  # !da & !ddin & nrdy & scsii
  # da & !db & !ddin & nrdy
  # bmt & !ddin & scsi & scsii
  # bmt & !ddin & drq & scsi
  # bmt & !ddin & scsi & slow

nrdy.d  =>
    !da & dc & !drq & nrdy & !scsii
  # !da & drq & nrdy & !scsii
  # !da & nrdy & scsii
  # !da & !db & !dc & !drq & nrdy & scsi & !scsii & !slow
  # da & !db & nrdy
  # db & !dc & nrdy
  # bmt & !da & !db & !dc & !nrdy & scsi & !slow
  # bmt & !da & !db & !dc & !nrdy & slow

dack.oe  =>   1
eop.oe  =>    1
```

Symbol Table

Pin Pol	Variable Name	Ext	Pin	Type	Pterms Used	Max Pterms	Min Level
	a22		9	V	-	-	-
	bclk		1	V	-	-	-
!	bmt		4	V	-	-	-
!	da		14	V	-	-	-
!	da	d	14	X	8	8	4
!	dack		12	V	2	7	4
!	db		15	V	-	-	-
!	db	d	15	X	2	8	4
!	dc		16	V	-	-	-
!	dc	d	16	X	5	8	4
!	ddin		5	V	-	-	-
	drq		7	V	-	-	-
!	eop		19	V	2	7	4
!	eprom		2	V	-	-	-
!	iord		17	V	-	-	-
!	iord	d	17	X	8	8	4
!	iowr		18	V	-	-	-
!	iowr	d	18	X	8	8	4
!	nrdy		13	V	-	-	-
!	nrdy	d	13	X	8	8	4
!	oe		11	V	-	-	-
!	scsi		3	V	-	-	-
	scsii		8	V	-	-	-
!	slow		6	V	-	-	-
	dack	oe	12	D	1	1	0
	eop	oe	19	D	1	1	0

LEGEND F : field D : default variable M : extended node
N : node I : intermediate variable T : function
V : variable X : extended variable U : undefined